

WHAT IS CLAIMED IS:

- 1 1. A method for providing row sense and row precharge currents to a memory,
2 comprising the steps of:
3 providing first current profiles for the row sense and row precharge currents
4 during normal memory accesses; and
5 providing a second current profile for at least one of the row sense and row
6 precharge currents during a memory refresh, the second current profile having less of
7 a current spike than the first profiles.
- 1 2. A method for providing row sense current to a memory, comprising the steps
2 of:
3 providing a first current profile for the row sense current during normal memory
4 accesses; and
5 providing a second current profile for the row sense current during a memory
6 refresh, the second current profile having less of a current spike than the first profile.
- 1 3. A method for providing row precharge current to a memory, comprising the
2 steps of:
3 providing a first current profile for the row precharge current during normal
4 memory accesses; and
5 providing a second current profile for the row precharge current during a
6 memory refresh, the second current profile having less of a current spike than the first
7 profile.
- 1 4. A method of refreshing a memory device, comprising the steps of: providing a
2 sequence of bank addresses for refreshing over an interface to the memory device;
3 and using an internal sequencer in the memory device to provide sequencing of row
4 addresses.
- 1 5. A method of refreshing a memory device, comprising the steps of:
2 providing a sequence of row addresses for refreshing the memory device; and
3 for each row, refreshing the row in a sequence of banks before refreshing a
4 subsequent row.

1 6. The method of claim 5 further comprising the steps of:
2 providing a sequence of bank addresses for refreshing over an interface to the
3 memory device; and
4 using an internal sequencer in the memory device to provide sequencing of
5 row addresses.

1 7. A method of refreshing a memory device, comprising the steps of:
2 simultaneously refreshing a plurality of banks.

1 8. A memory device comprising:
2 a memory array;
3 a plurality of sense amplifiers connected to the memory array;
4 a control circuit connected to the sense amplifiers, the control circuit being
5 configured to control the sense amplifiers to:
6 provide first current profiles for row sense currents during normal
7 memory accesses; and
8 provide second current profiles for the row sense currents during a
9 memory refresh, the second current profiles having less of a current spike than
10 the first profiles.

1 9. The memory device of claim 8 further comprising:
2 a plurality of sense amplifier driver transistors;
3 wherein the control circuit provides a drive signal to the driver transistors using
4 a reduced slew rate for a memory refresh.

1 10. The memory device of claim 8 further comprising:
2 a plurality of sense amplifier driver transistors;
3 wherein the control circuit provides a drive signal to the driver transistors using
4 a lower drive voltage for a memory refresh than for other memory operations.

1 11. The memory device of claim 8 further comprising:
2 a plurality of sense amplifier driver transistors connected in parallel;

3 wherein the control circuit sequentially turns on the driver transistors for a
4 memory refresh.

1 12. A memory device comprising:
2 a memory array;
3 a plurality of row precharge drivers connected to the memory array;
4 a control circuit connected to the row precharge drivers, the control circuit
5 being configured to control the row precharge drivers to
6 provide first current profiles for row precharge currents during normal
7 memory accesses; and
8 provide second current profiles for the row precharge currents during a
9 memory refresh, the second current profiles having less of a current spike than
10 the first profiles.

1 13. The memory device of claim 12 further comprising:
2 a plurality of row precharge driver transistors;
3 wherein the control circuit provides a drive signal to the driver transistors using
4 a reduced slew rate for a memory refresh.

1 14. The memory device of claim 12 further comprising:
2 a plurality of row precharge driver transistors;
3 wherein the control circuit provides a drive signal to the driver transistors using
4 a lower drive voltage for a memory refresh.

1 15. The memory device of claim 12 further comprising:
2 a plurality of row precharge driver transistors connected in parallel;
3 wherein the control circuit sequentially turns on the driver transistors for a
4 memory refresh.

1 16. A memory device comprising:
2 an internal sequencer configured to provide sequencing of row addresses for
3 each of a plurality of banks in the memory device; and

4 an interface circuit configured to receive a sequence of bank addresses for
5 refreshing over an interface, and provide enabling control signals to the internal
6 sequencer.

1 17. A method of refreshing a memory device, comprising the steps of:
2 at one of a plurality of clock rates, selected in accordance with a device
3 configuration signal:
4 internally generating a sequence of row addresses for refreshing the
5 memory device; and
6 refreshing a row of the memory device associated with a currently
7 generated row address.

1 18. The method of claim 17 wherein the device configuration signal is set by
2 determining a worst case memory cell hold time for memory cells in the memory
3 device and setting the device configuration signal in accordance with the determined
4 worst case memory cell hold time.

1 19. A memory device, comprising:
2 a memory array;
3 a plurality of sense amplifiers connected to the memory array; and
4 a control circuit connected to the sense amplifiers, the control circuit being
5 configured to control the sense amplifiers to refresh memory cells in the memory
6 array, one row at a time, at one of a plurality of clock rates, selected in accordance
7 with a device configuration signal.

1 20. The memory device of claim 19 wherein the control circuit includes a row
2 address counter, and the device configuration signal is a permanently set signal,
3 having one of a plurality number of predefined values, that determines which of a like
4 plurality of clock signals are used to increment the row address counter and to initiate
5 a row refresh operation.